BF2 Data sheet

LeapFive

Release Date: 6 Aug 2020

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1 Overview

LF688/LF686 is Wi-Fi + BLE combo chipset for ultra-low-power application.

Wireless subsystem contains 2.4G radio, Wi-Fi 802.11b/g/n and Bluetooth LE 5.0 baseband/MAC designs. Microcontroller subsystem contains a low-power 32-bit RISC CPU, high-speed cache and memories. Power Management Unit controls low-power modes. Moreover, variety of security features are supported.

Peripheral interfaces include SDIO, SPI, UART, I2C, IR remote, PWM, ADC, ACOMP, ACOMP, DAC, PIR, and GPIOs.

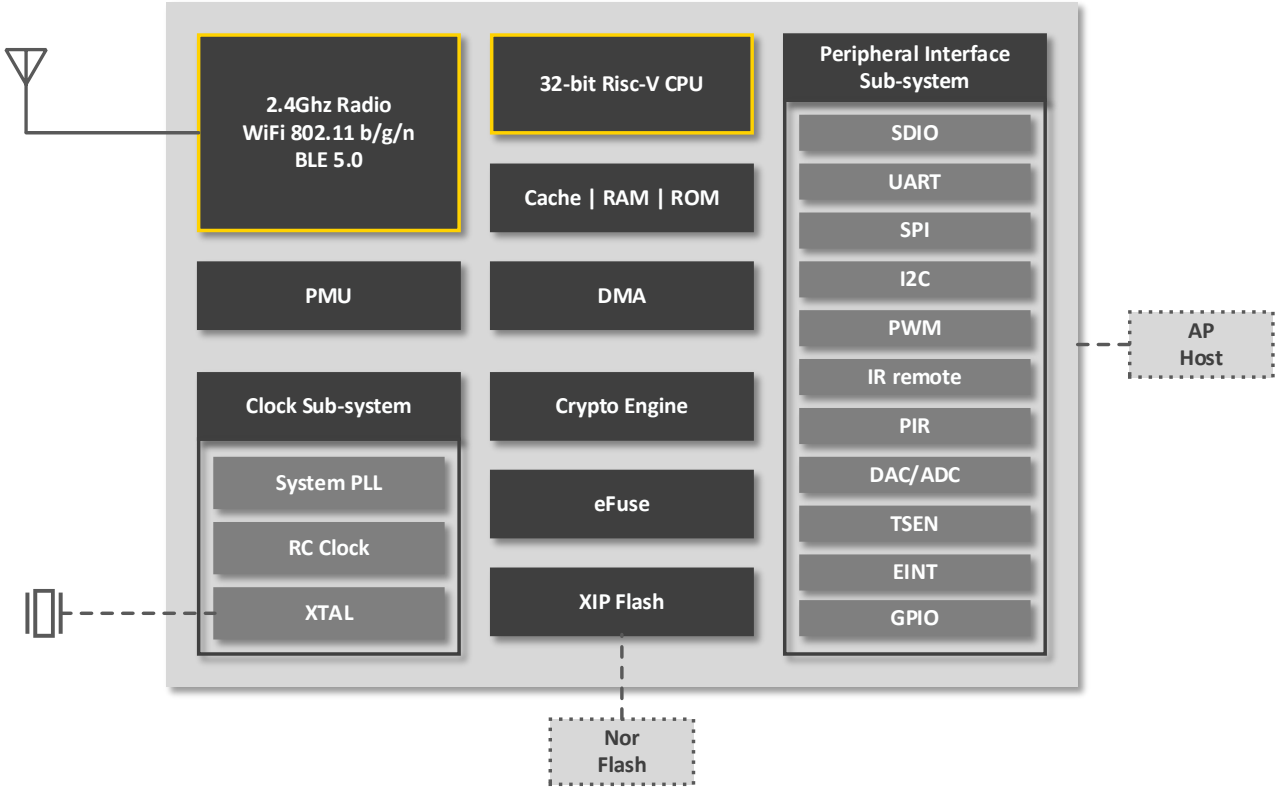


Figure 1 Block Diagram

1.1 Wireless

- 2.4 GHz RF transceiver
- Wi-Fi 802.11 b/g/n
- Bluetooth® Low Energy 5.0
  BLE 5.0 Channel Selection#2 is supported
  2M PHY / Coded PHY / ADV extension is not supported
- Wi-Fi 20MHz bandwidth
- Wi-Fi Security WPS / WEP / WPA / WPA2 Personal / WPA2 Enterprise / WPA3
- STA, SoftAP and sniffer modes
- Multi-cloud connectivity
- Wi-Fi fast connection with BLE assistance
- Wi-Fi and BLE coexistence
- Integrated balun, PA/LNA

1.2 MCU Subsystem

- 32-bit RISC CPU with FPU (floating point unit)
- Level-1 cache
- One RTC timer up to one year
- Two 32b general purpose timers
- Four DMA channels
- DFS (dynamic frequency scaling) from 1MHz to 192MHz
- JTAG development support
- XIP QSPI Flash with hardware encryption support

1.3 Memory

- 276KB SRAM
- 128KB ROM
- 1Kb eFuse
- Embedded Flash (Optional)

1.4 Security

- Secure boot
- Secure debug ports
- QSPI Flash On-The-Fly AES Decryption (OTFAD) - AES-128, CTR mode
- AES 128/192/256 bits
- SHA-1/224/256
- TRNG (True Random Number Generator)
- PKA (Public Key Accelerator)

1.5 Peripheral

- One SDIO 2.0 slave
- One SPI master/slave
- Two UART
- One I2C master/slave
- Five PWM channels
- 10-bit general DAC
- 12-bit general ADC
- Two general analog comparators (ACOMP)
- PIR (Passive Infra-Red) detection
- IR remote HW accelerator
- 16 or 23 GPIOs

1.6 Power Management

- Off
- Hibernate (flexible modes)
- Power Down Sleep (flexible modes)
- Active

1.7 Clock

- Support XTAL 24/26/32/38.4/40MHz
- Internal RC 32KHz oscillator
- Internal RC 32MHz oscillator
- Internal System PLL

2 Functional Description

LF688/LF686 main functions described as follows

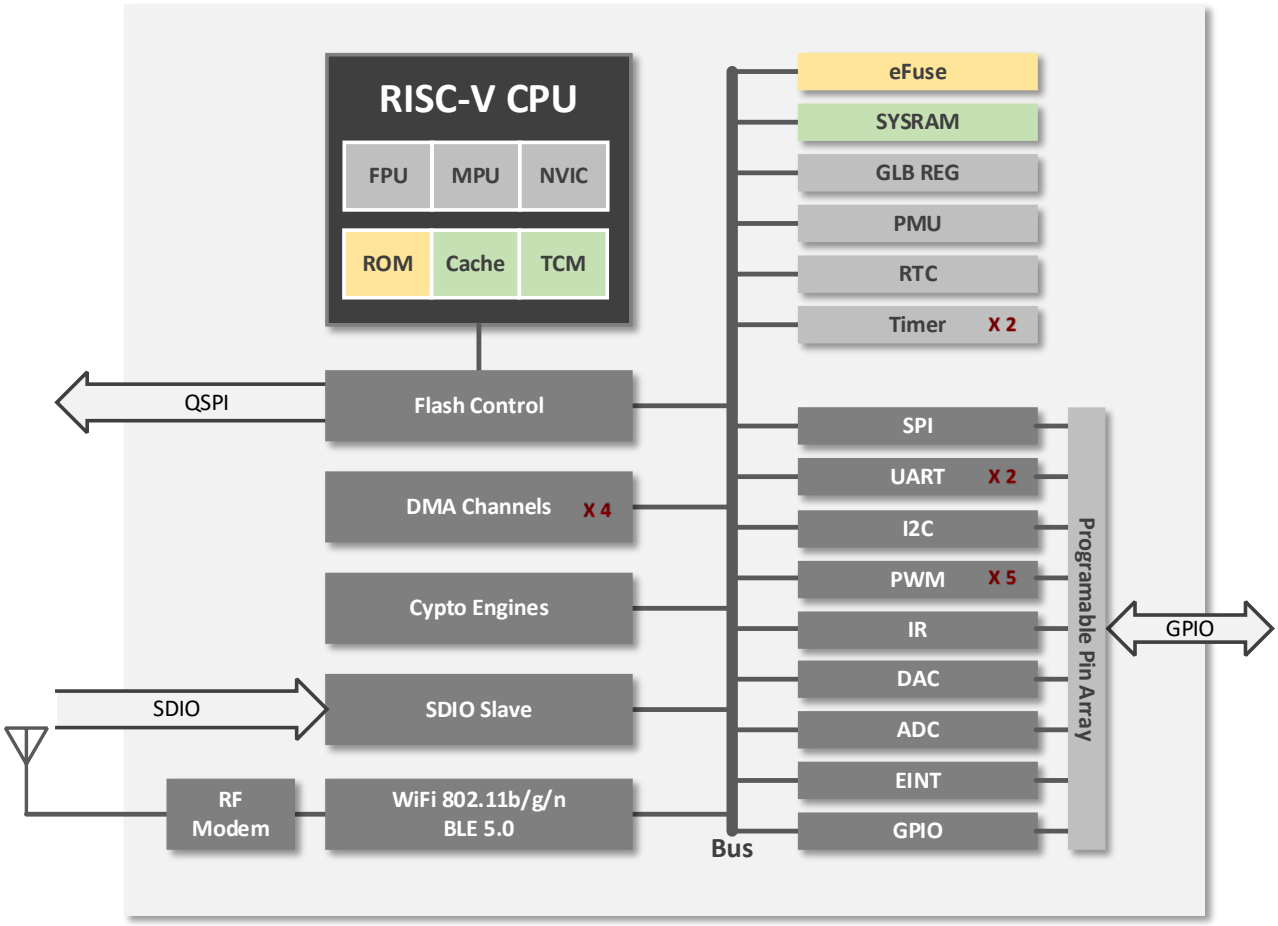


Figure 2 System Architecture

2.1 CPU

LF688/LF686 32-bit RISC CPU contains FPU (floating-point unit) for 32-bit single-precision arithmetic, three-stage pipelined (IF, EXE, WB), compressed 16 and 32-bit instruction set, standard JTAG debugger port including 4 hardware-programmable breakpoints, interrupt controller including 64 interrupts and 16 interrupt levels/priorities for low latency interrupt processing. Up to 192MHz clock frequency, can be dynamically configured to change clock frequency, enter the power saving mode to achieve low power consumption.

Both WiFi/BLE stack and application run on single 32-bit RISC CPU for simple and ultra-low power applications. CPU performance ~1.46 DMIPS/MHz. ~3.1 CoreMark/MHz.

2.2 Cache

LF688/LF686 cache improves CPU performance to access external memory. Cache memories can be partially or fully configured as TCM (tightly coupled memory).

2.3 Memory

LF688/LF686 memories include: on-chip zero-delay SRAM memories, read-only memories, write-once memories, embedded flash memory (optional)

2.4 DMA

LF688/LF686 DMA (direct memory access) controller has four dedicated channels that manage data transfer between peripherals and memories to improve cpu/bus efficiency. There are three main types of transfers including memory to memory, memory to peripheral, and peripheral to memory. DMA also supports LLI (link list item) that multiple transfers are pre-defined by a series of linked lists, then hardware automatically complete all transfers according to each LLI size and address. DMA supports peripheral UART, I2C, SPI, ADC and DAC.

2.5 Bus

LF688/LF686 bus fabric connection and memory-map summarized as follows

Table 3 Bus Connection

Master / Slave	CPU	SDIO	Crypto Engine	DMA	Debug
SRAM	V	V	V	V	V
Peripheral	V	V	-	V	V
WiFi/BLE	V	V	-	V	V

Table 4 Memory Map

Module	Base Address	Size	Description
WRAM	0x42030000	112KB	Wireless SRAM memory
RETRAM	0x40010000	4KB	Deep sleep memory (Retention RAM)
HBN	0x4000F000	4KB	Deep sleep control (Hibernate)
PDS	0x4000E000	4KB	Sleep control (Power Down Sleep)
SDU	0x4000D000	4KB	SDIO control
DMA	0x4000C000	4KB	DMA control
QSPI	0x4000B000	4KB	Flash/pSRAM control
IRR	0x4000A600	256B	IR Remote control
TIMER	0x4000A500	256B	Timer control
PWM	0x4000A400	256B	Pulse Width Modulation *5 control
I2C	0x4000A300	256B	I2C control
SPI	0x4000A200	256B	SPI master/slave control
UART1	0x4000A100	256B	UART control
UART0	0x4000A000	256B	UART control
L1C	0x40009000	4KB	Cache control
eFuse	0x40007000	4KB	eFuse memory control
TZ2	0x40006000	4KB	Trust isolation
TZ1	0x40005000	4KB	Trust isolation
SEC	0x40004000	4KB	Security engine
GPIP	0x40002000	4KB	General purpose DAC/ADC/ACOMP interface control
MIX	0x40001000	4KB	Mixed signal register
GLB	0x40000000	4KB	Global control register
RAM	0x22020000	64KB	On-chip memory
XIP	0x23000000	16MB	XIP Flash memory
DTCM	0x22014000	48KB	Data cache memory
ITCM	0x22008000	48KB	Instruction cache memory
ROM	0x21000000	128KB	Read-only memory

2.6 Interrupt

LF688/LF686 supports internal RTC wake-up and external interrupts wake-up.
CPU interrupt controller supports stack/nesting, level/pulse, and high/low active.

2.7 Boot

LF688/LF686 supports multiple boot options: UART, SDIO, and Flash.

2.8 Power

PMU (power management unit) manages the power of the entire chip and is divided into active, idle, sleep, and hibernate power modes. The software can be configured to enter sleep mode and wake-up via RTC timer or EINT to achieve low-power sleep and accurate wake-up management.

Power down sleep modes are flexible for applications to configure as the lowest power consumption.

2.9 Clock

Clock control unit generates clocks to the core MCU and the peripheral SOC devices. The root clock source can be XTAL, PLL or RC oscillator. Dynamic power-saved by proper configurations such as sel, div, en, etc. PMU runs at 32KHz clock to keep system low-power in sleep mode.

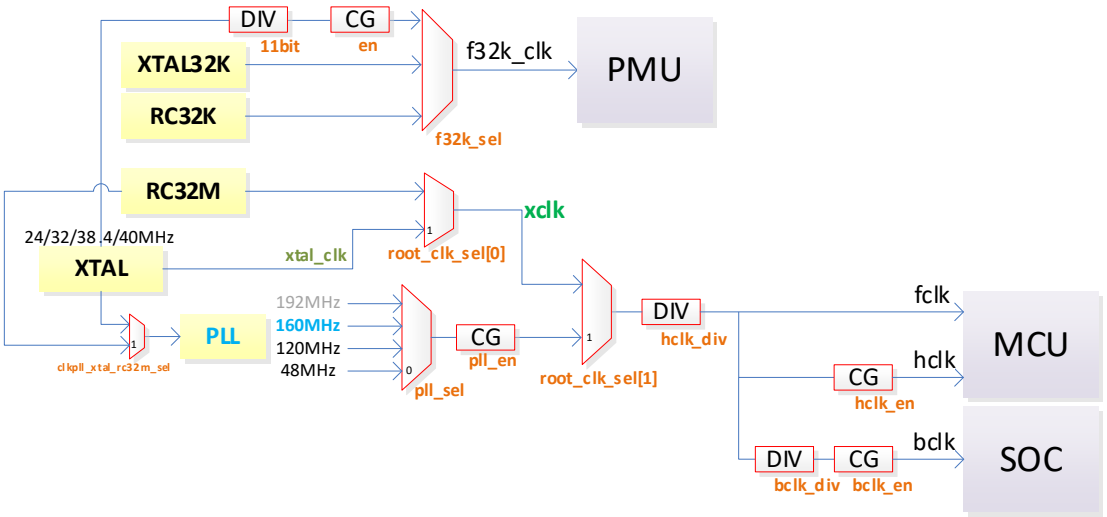


Figure 5 Clock Architecture

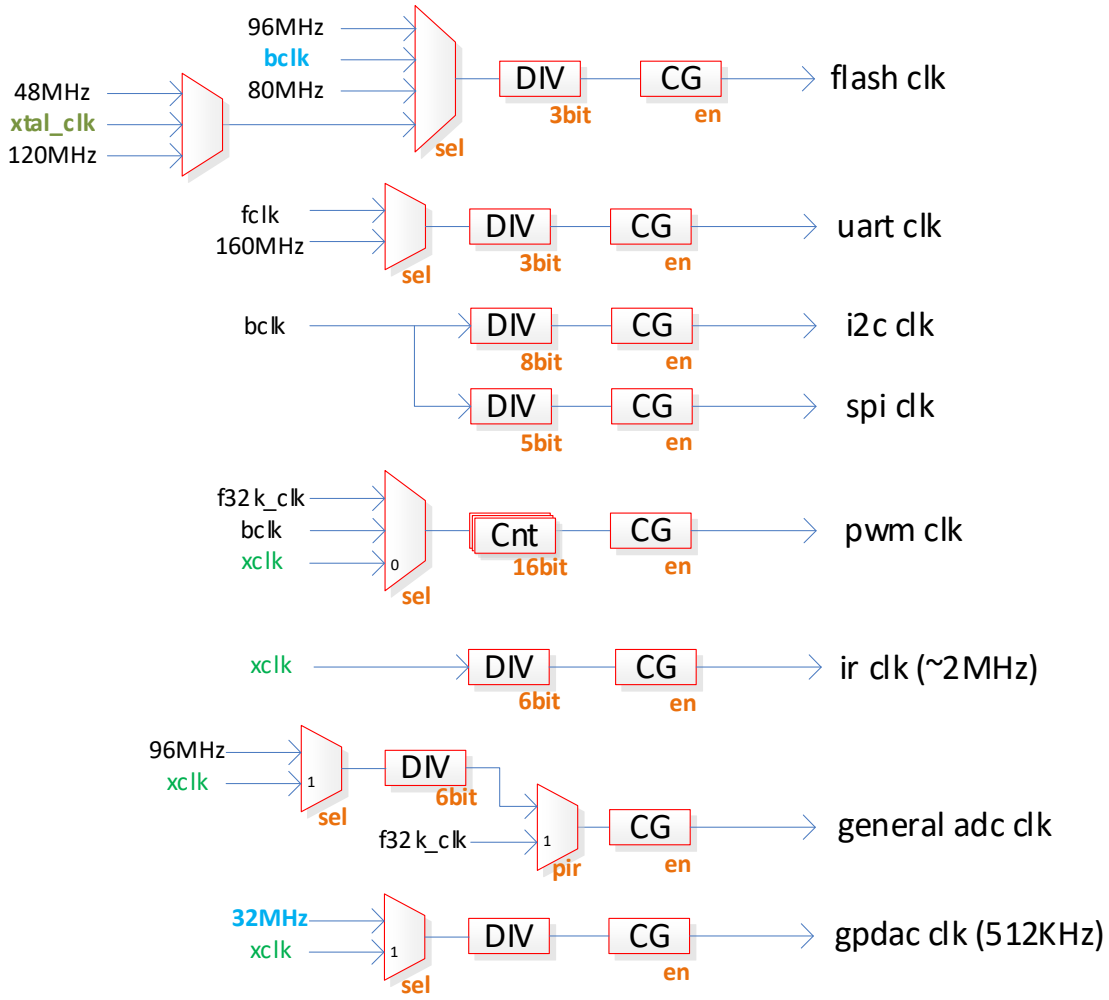


Figure 6 SoC Peripheral Clock

2.10 Peripherals

Peripherals include SDIO, SPI, UART, I2C, IR remote, PWM, ADC, ACOMP, DAC, PIR.

Each peripheral can be assigned to different groups of GPIOs through flexible configurations.

Each GPIO can be used as a general-purpose input and output function.

3 Pin Definition (QFN32)

LF686 32-pin package includes 10 power pins, 6 analog pins, and 16 flexible GPIO pins.

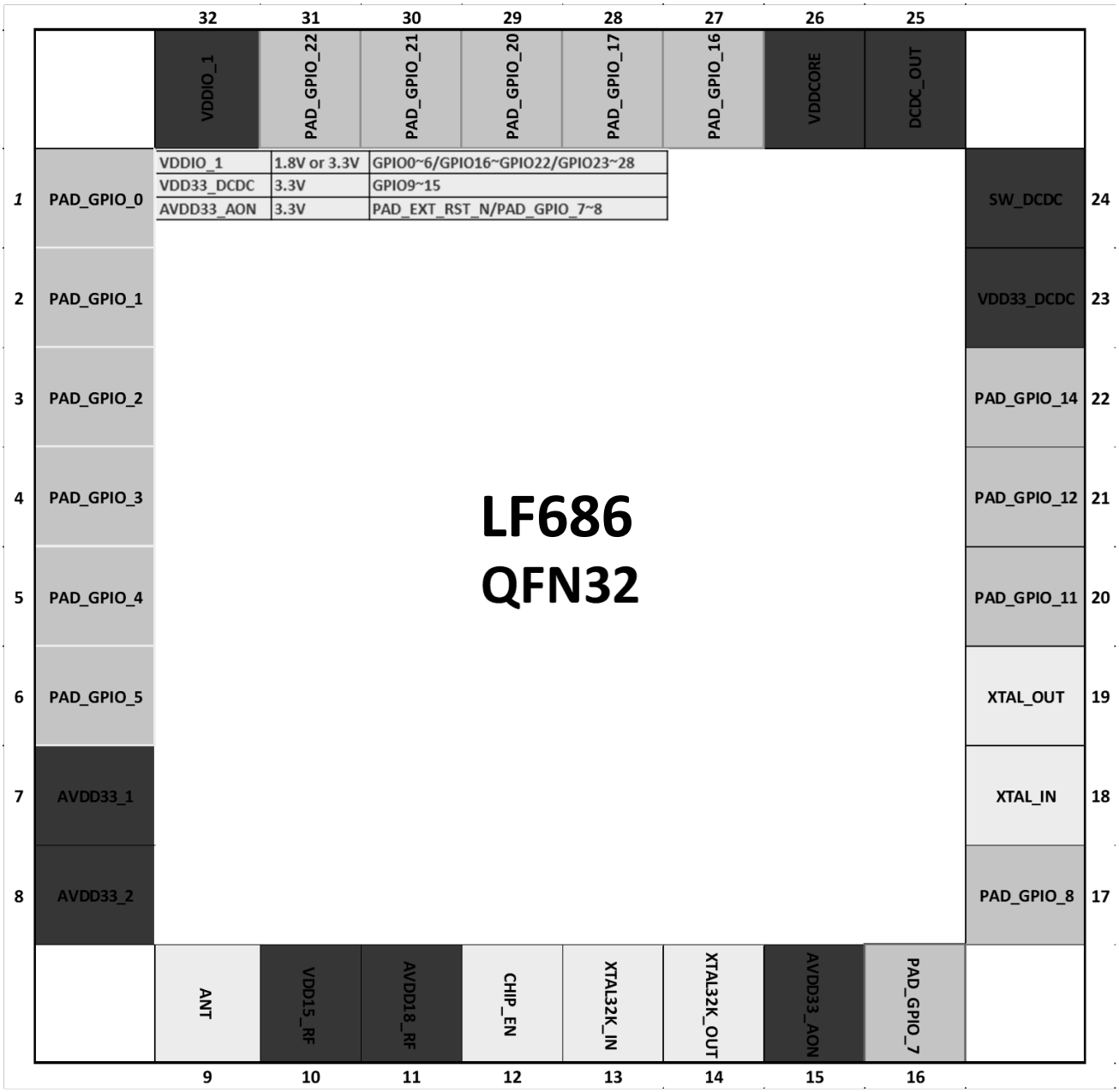


Figure 7 Pin Top View (QFN32)

Table 8 Pin Description (QFN32)

No.	Name	Type	Description
1	PAD_GPIO_0	Digital	SDIO, SFLASH, SPI, I2C, UART, PWM, GPIO
2	PAD_GPIO_1	Digital	SDIO, SFLASH, SPI, I2C, UART, PWM, GPIO
3	PAD_GPIO_2	Digital	SDIO, SFLASH, SPI, I2C, UART, PWM, GPIO
4	PAD_GPIO_3	Digital	SDIO, SPI, I2C, UART, PWM, GPIO
5	PAD_GPIO_4	Digital	SDIO, SPI, I2C, UART, PWM, ADC, ACOMP, GPIO
6	PAD_GPIO_5	Digital	SDIO, SPI, I2C, UART, PWM, ADC, ACOMP, GPIO
7	AVDD33_1	Power	Externally powered 3.3V
8	AVDD33_2	Power	Externally powered 3.3V
9	ANT	Analog	RF input and output (single pin)
10	VDD15_RF	Power	RF power 1.5V
11	AVDD18_RF	Power	RF power 1.8V
12	CHIP_EN	Digital	Chip enable
13	XTAL32K_IN	Analog	Crystal oscillator 32.768KHz input
14	XTAL32K_OUT	Analog	Crystal oscillator 32.768KHz output
15	AVDD33_AON	Power	Externally powered 3.3V
16	PAD_GPIO_7	Digital	SPI, I2C, UART, PWM, GPIO
17	PAD_GPIO_8	Digital	SPI, I2C, UART, PWM, GPIO
18	XTAL_IN	Analog	External crystal input, support 24/26/32/38.4/40MHz
19	XTAL_OUT	Analog	External crystal output, support 24/26/32/38.4/40MHz
20	PAD_GPIO_11	Digital	SPI, I2C, UART, PWM, ADC, GPIO
21	PAD_GPIO_12	Digital	SPI, I2C, UART, PWM, ADC, ACOMP, GPIO
22	PAD_GPIO_14	Digital	SPI, I2C, UART, PWM, ADC, ACOMP, DAC, GPIO
23	VDD33_DCDC	Power	DCDC
24	SW_DCDC	Power	DCDC
25	DCDC_OUT	Power	DCDC
26	VDDCORE	Power	Core Power
27	PAD_GPIO_16	Digital	SPI, I2C, UART, PWM, GPIO
28	PAD_GPIO_17	Digital	SFLASH, SPI, I2C, UART, PWM, GPIO
29	PAD_GPIO_20	Digital	SFLASH, SPI, I2C, UART, PWM, GPIO
30	PAD_GPIO_21	Digital	SFLASH, SPI, I2C, UART, PWM, GPIO
31	PAD_GPIO_22	Digital	SFLASH, SPI, I2C, UART, PWM, GPIO
32	DVDDIO_1	Power	Externally powered 3.3V or 1.8V

4 Pin Definition (QFN40)

LF688 40-pin package includes 10 power pins, 6 analog pins, 1 reset pin, and 23 flexible GPIO pins.

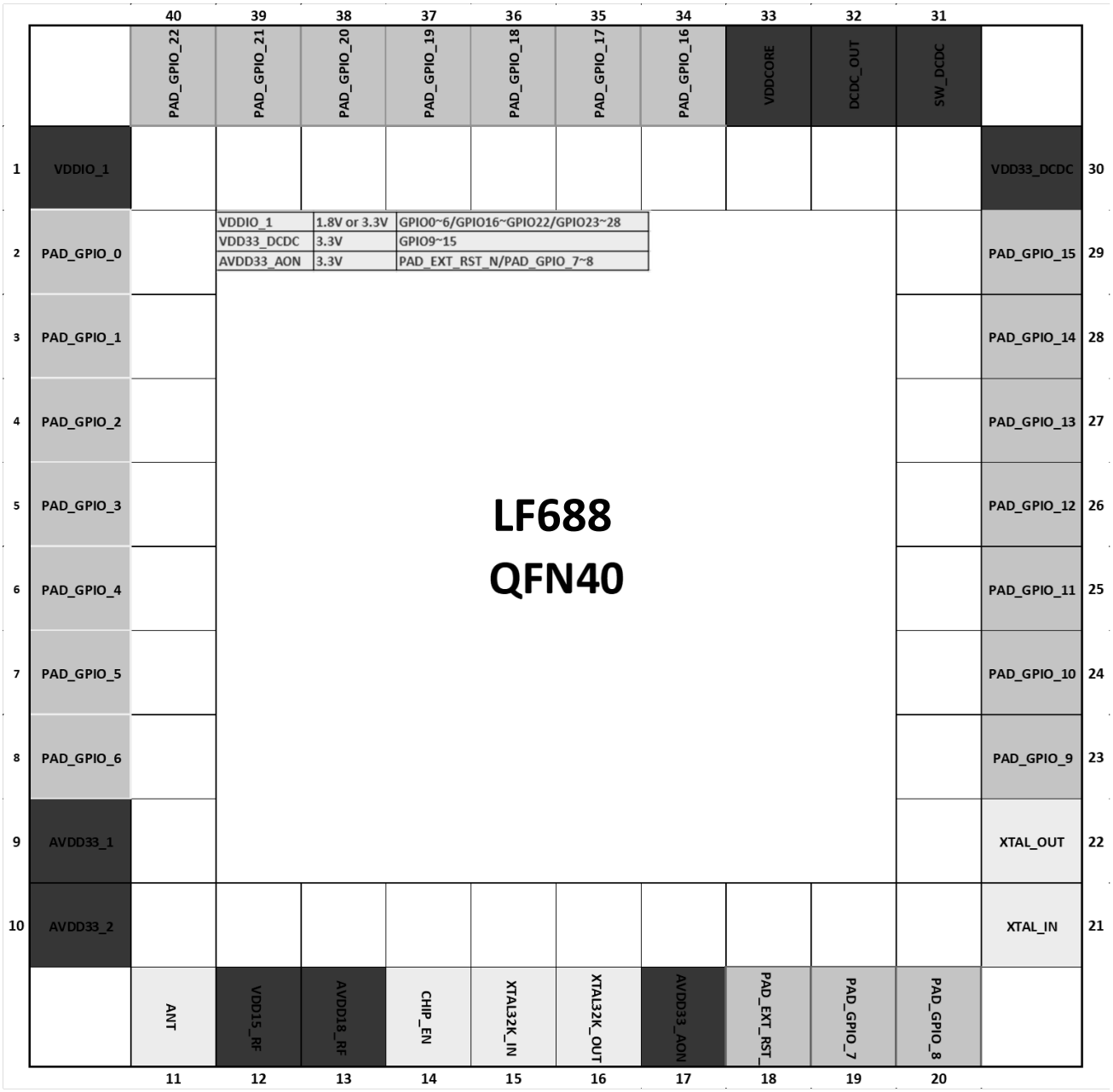


Figure 9 Pin Top View (QFN40)

Table 10 Pin Description (QFN40)

No.	Name	Type	Description
1	DVDDIO_1	Power	Externally powered 3.3V or 1.8V
2	PAD_GPIO_0	Digital	SDIO, SFLASH, SPI, I2C, UART, PWM, GPIO
3	PAD_GPIO_1	Digital	SDIO, SFLASH, SPI, I2C, UART, PWM, GPIO
4	PAD_GPIO_2	Digital	SDIO, SFLASH, SPI, I2C, UART, PWM, GPIO
5	PAD_GPIO_3	Digital	SDIO, SPI, I2C, UART, PWM, GPIO
6	PAD_GPIO_4	Digital	SDIO, SPI, I2C, UART, PWM, ADC, ACOMP, GPIO
7	PAD_GPIO_5	Digital	SDIO, SPI, I2C, UART, PWM, ADC, ACOMP, GPIO
8	PAD_GPIO_6	Digital	SPI, I2C, UART, PWM, ADC, ACOMP, GPIO
9	AVDD33_1	Power	Externally powered 3.3V
10	AVDD33_2	Power	Externally powered 3.3V
11	ANT	Analog	RF input and output (single pin)
12	VDD15_RF	Power	RF power 1.5V
13	AVDD18_RF	Power	RF power 1.8V
14	CHIP_EN	Digital	Chip enable
15	XTAL32K_IN	Analog	Crystal oscillator 32.768KHz input
16	XTAL32K_OUT	Analog	Crystal oscillator 32.768KHz output
17	AVDD33_AON	Power	Externally powered 3.3V
18	PAD_EXT_RST	Digital	External reset
19	PAD_GPIO_7	Digital	SPI, I2C, UART, PWM, GPIO
20	PAD_GPIO_8	Digital	SPI, I2C, UART, PWM, GPIO
21	XTAL_IN	Analog	External crystal input, support 24/26/32/38.4/40MHz
22	XTAL_OUT	Analog	External crystal output, support 24/26/32/38.4/40MHz
23	PAD_GPIO_9	Digital	SPI, I2C, UART, PWM, ADC, ACOMP, GPIO
24	PAD_GPIO_10	Digital	SPI, I2C, UART, PWM, ADC, GPIO
25	PAD_GPIO_11	Digital	SPI, I2C, UART, PWM, ADC, GPIO
26	PAD_GPIO_12	Digital	SPI, I2C, UART, PWM, ADC, ACOMP, GPIO
27	PAD_GPIO_13	Digital	SPI, I2C, UART, PWM, ADC, ACOMP, DAC, GPIO
28	PAD_GPIO_14	Digital	SPI, I2C, UART, PWM, ADC, ACOMP, DAC, GPIO
29	PAD_GPIO_15	Digital	SPI, I2C, UART, PWM, ADC, GPIO
30	VDD33_DCDC	Power	DCDC
31	SW_DCDC	Power	DCDC
32	DCDC_OUT	Power	DCDC
33	VDDCORE	Power	Core Power
34	PAD_GPIO_16	Digital	SPI, I2C, UART, PWM, GPIO
35	PAD_GPIO_17	Digital	SFLASH, SPI, I2C, UART, PWM, GPIO
36	PAD_GPIO_18	Digital	SFLASH, SPI, I2C, UART, PWM, GPIO
37	PAD_GPIO_19	Digital	SFLASH, SPI, I2C, UART, PWM, GPIO
38	PAD_GPIO_20	Digital	SFLASH, SPI, I2C, UART, PWM, GPIO
39	PAD_GPIO_21	Digital	SFLASH, SPI, I2C, UART, PWM, GPIO
40	PAD_GPIO_22	Digital	SFLASH, SPI, I2C, UART, PWM, GPIO

5 RF Characteristic

RF Characteristics of Receiving and Transmitting modes.

Table 11 RX RF Characteristics

Mode		Note	Performance @25 ^{O}C			
			Min.	Typ	Max.	Unit
RX Sensitivity	11b - 1Mbps			-98		dBm
	11b - 11Mbps			-91		
	11g - 6Mbps			-93		
	11g - 54Mbps			-77		
	11n - MCS0			-93		
	11n - MCS7			-73		
Maximum RX Level	11b - 1Mbps			5		
	11n - MCS0			-4		
	11n - MCS7			-13		
Adjacent Channel Rejection	11b - 1Mbps			40		dB
	11b - 11Mbps			40		
	11g - 6Mbps			36		
	11g - 54Mbps			22		
	11n - MCS0			36		
	11n - MCS7			19		
S11				<-10		

Table 12 TX RF Characteristics

Mode		Note	Performance @25 ^{O}C			
			Min.	Typ	Max.	Unit
TX Power	11b - 1Mbps			21		dBm
	11b - 11Mbps			21		
	11g - 6Mbps			19		
	11g - 54Mbps			18		
	11n - MCS0			19		
	11n - MCS7			17		
TX EVM	11g - 54Mbps			-28		dB
	11n - MCS7			-28		

6 Power Consumption

Power Consumption of each power mode.

Table 13 Power Modes & Whole-chip Current

Mode		Note	Power @25 ^{O}C			
			Min.	Typ	Max.	Unit
RX	11b			35		mA
	11g			39		
	11n			39		
TX	11b - 11Mbps @21dBm	Duty 50%		190		
		Duty 99%		310		
	11g - 54Mbps @18dBm	Duty 50%		145		
		Duty 99%		230		
	11n - MCS7 @17dBm	Duty 50%		130		
		Duty 99%		215		
MCU	Run	Freq@192MHz		22		
	Standby	Freq@<10MHz		2		
Sleep	PDS7	Fast recover		12		uA
Hibernate	HBN	RTC or GPIO wakeup		0.5		
Shut-down				0.1		

7 Electrical Specifications

7.1 Absolute Maximum Rating

Table 14 Absolute Maximum Rating

Symbol	Min.	Max.	Unit
AVDD33_1	-0.3	3.63	V
AVDD33_2	-0.3	3.63	V
AVDD33_AON	-0.3	3.63	V
DVDD33_DCDC	-0.3	3.63	V
DVDDIO_1	-0.3	3.63	V
ESD Protection (HBM)		*2000*	*V*
Storage Temperature	*-45*	*135*	^{O}C

7.2 Operating Condition

Table 15 Recommended Power Operating Range

Pin Name	Min.	Typ	Max.	Unit
AVDD33_1	2.1	3.3	3.63	V
AVDD33_2	2.1	3.3	3.63	V
AVDD33_AON	2.1	3.3	3.63	V
DVDD33_DCDC	2.1	3.3	3.63	V
DVDDIO_1	2.1 / 1.62	3.3 / 1.8	3.63 / 1.98	V

Table 16 Recommended Temperature Operating Range

Item		Min.	Max.	Unit
Temperature	Main Die	*-30*	*105*	^{O}C
	Multi-Die SiP	*-30*	*85*	^{O}C

Table 17 General Operating Conditions

Item	Description	Min.	Typ	Max.	Unit
F_{CPU}	CPU/TCM/Cache clock frequency	0	50	192	MHz
F_{SYS}	System clock frequency	0	50	96	MHz

8 Reference Design (simplified)

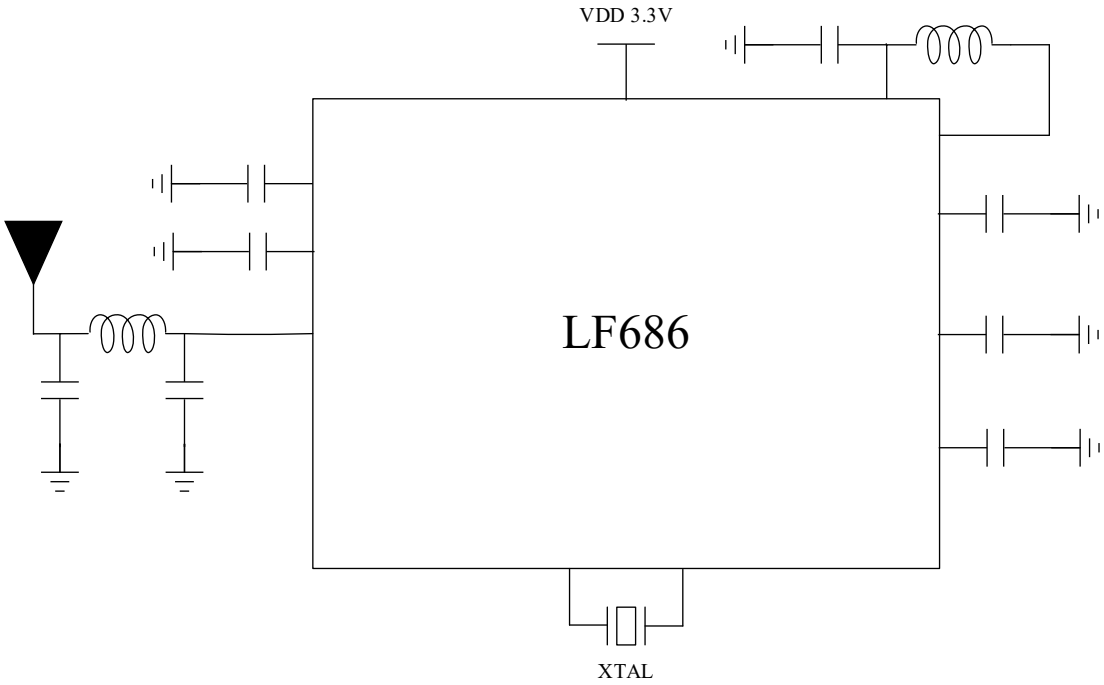
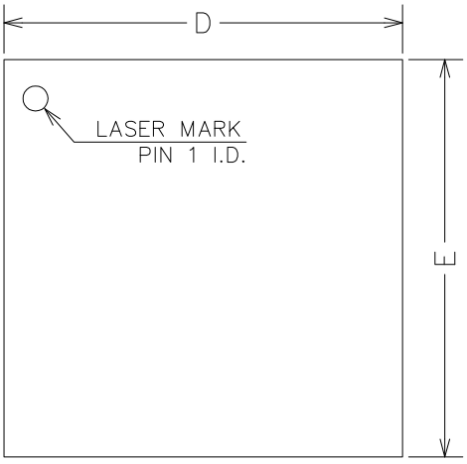


Figure 18 Reference Design

9 Package Information (QFN32 4x4)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H		0.30REF	
K		0.25REF	
L	0.25	0.30	0.35
R	0.09	–	–
c1	–	0.10	–
c2	–	0.10	–

Figure 19 QFN32 Top View

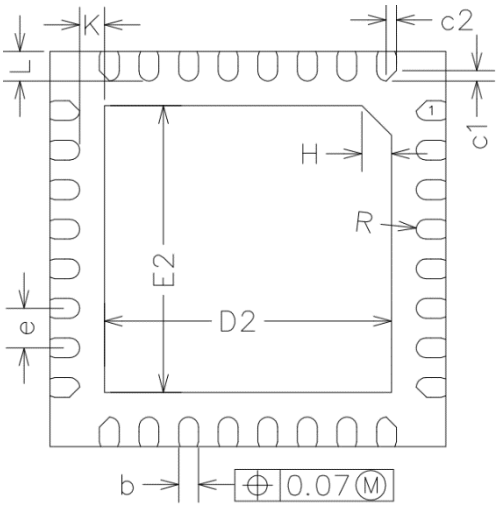


Figure 20 QFN32 Bottom View

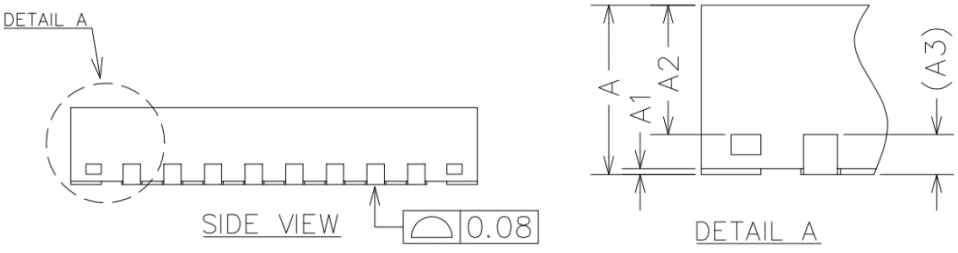
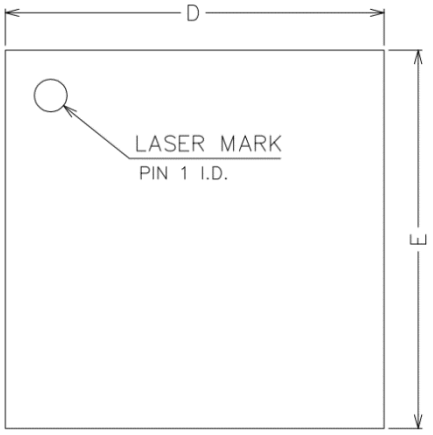


Figure 21 QFN32 Side View

10 Package Information (QFN40 5x5)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20REF	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	–	–
L	0.35	0.40	0.45
R	0.075	–	–
C1	–	0.12	–
C2	–	0.12	–

Figure 22 QFN40 Top View

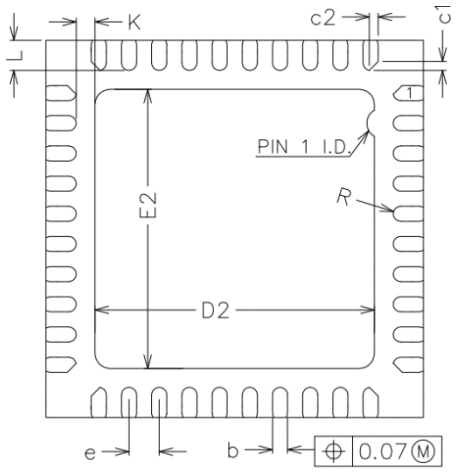


Figure 23 QFN40 Bottom View

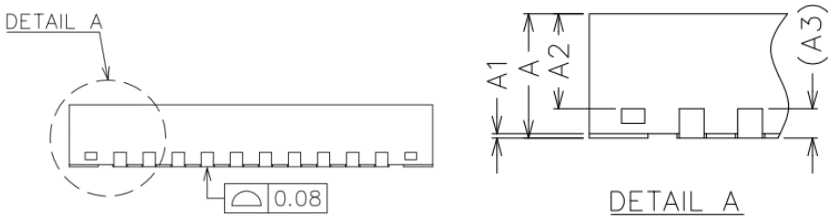


Figure 24 QFN40 Side View

11 Top Marking Definition

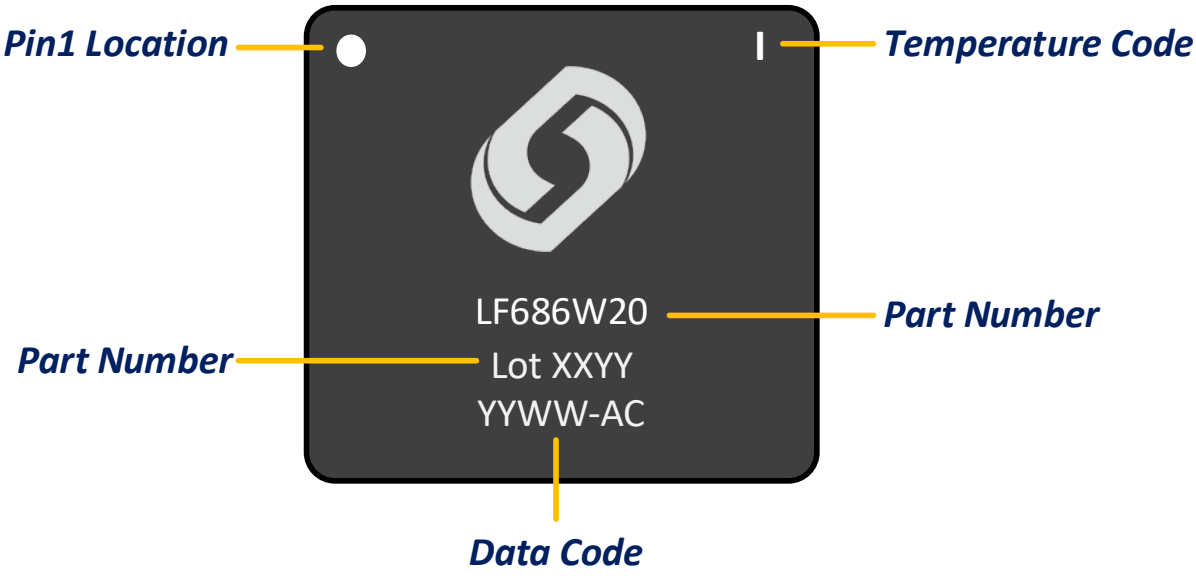


Figure 25 Top Marking Definition

12 Ordering Information

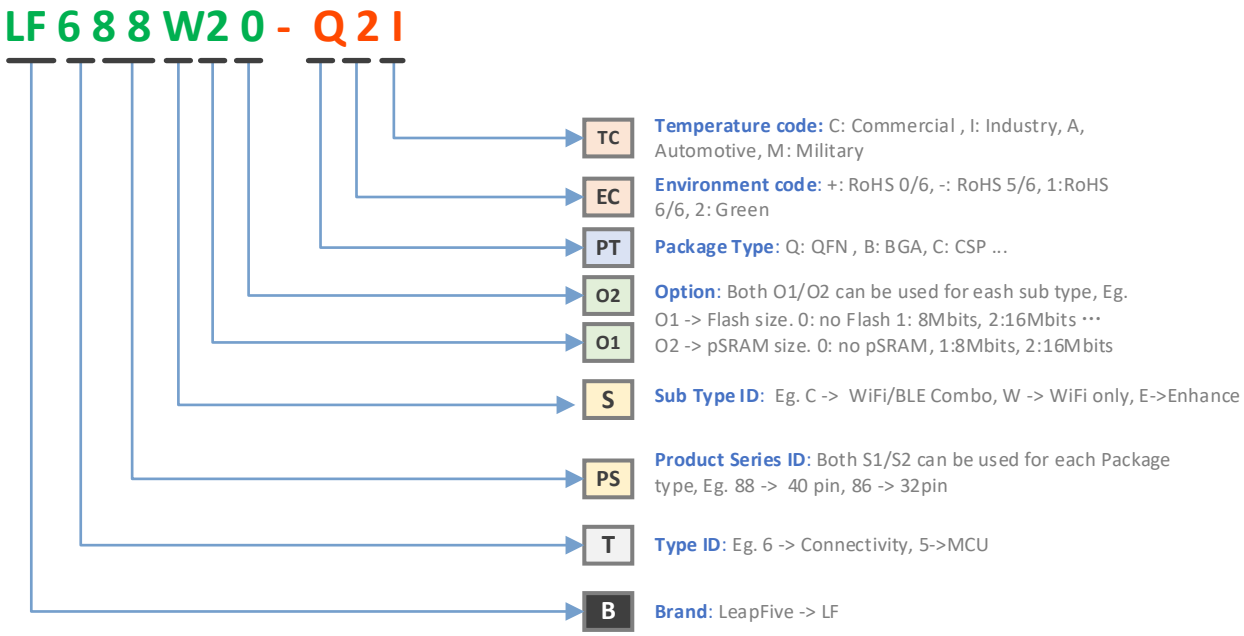


Figure 26 Part Number

Table 27 Part Order Options

Product No.	Description
LF686W-00-Q2I	WiFi, QFN32
LF686W-20-Q2I	WiFi, QFN32, flash 16Mb
LF686C-00-Q2I	WiFi/BLE Combo, QFN40
LF686C-20-Q2I	WiFi/BLE Combo, QFN40, flash 16Mb
LF688W-00-Q2I	WiFi, QFN40
LF688W-20-Q2I	WiFi, QFN40, flash 16Mb
LF688C-00-Q2I	WiFi/BLE Combo, QFN40
LF688C-20-Q2I	WiFi/BLE Combo, QFN40, flash 16Mb